increases in temperature and transfer heat to said adhesive substrate, said interposer and said solder balls, causing solder balls to reach a liquid state;

separately controlling the temperature of said interposer in order to minimize differences in thermal expansion;

removing said energy such that all said contacts form physical bonds and said solder balls cool and harden, forming physical bonds between said solder balls and said ports;

removing said polymer film; and

separating the resulting composite structure into discrete chips.

Add claims 19 and 20:

19. A method as in claim 14, further including the step of preheating said interposer prior to alignment with the wafer.

20. A method as in claim 15, further including the step of preheating said interposer prior to alignment with the wafer.

Remarks

Favorable reconsideration and allowance of the application are respectfully requested in view of the above amendments the following comments.

The rejection of claims 14-18 as unpatentable over Arima, et al. in view of Khandros, et al. is respectfully traversed, since the references fail to disclose or suggest the subject matter of the invention as defined by the claims. More specifically, the references do not show what the Examiner claims they show.

For example, Arima chips 9 are not "a semiconductor wafer" comprising a plurality

of circuit chips, as required by applicants' claims. Instead, each is a single discrete circuit chip. This is a critical difference, rendering all other portions of Arima remote and irrelevant.

Further, applicants' method includes the step of applying radiant energy to effect reflow of the solder balls, which ensures selective heating of the silicon; and enables separate control of interposer temperatures at lower levels, to minimize differences in thermal expansion. No such step is suggested in Arima, and indeed no such CTE mismatch problem arises in Arima, since chips 9 of Arima are not part of an undivided wafer, as required by applicants' claims.

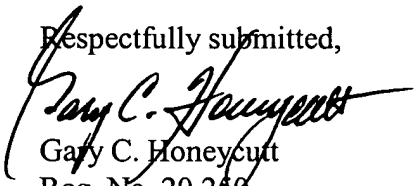
Still further, applicants' claim 15 includes a specific range of wavelengths for radiant heating, thereby ensuring maximum selective absorption of heat by the semiconductor, leaving the substrate at lower temperatures. No such step is suggested by the references.

Also, applicants' claims 19 and 20 include the step of preheating the interposer prior to the alignment. See page 15, lines 1-9 of applicants' specification. No such step is suggested by the references.

Khandros is cited to show "a planarized array of solder balls" attached to exit ports. But in fact Khandros does not describe any such planarization of solder balls, and of course Khandros fails to address the above-noted deficiencies of Arima.

For all the above reasons, the rejection is improper and should be withdrawn.

Respectfully submitted,



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11. The semiconductor assembly of Claim 1 wherein said electrically insulating interposer comprises ceramic material.

12. The semiconductor assembly of Claim 1 wherein said electrically conductive paths comprise gold or copper when said electrically insulating interposer is organic material, and comprise tungsten or tungsten alloy when said insulating interposer is ceramic.

13. The semiconductor assembly of Claim 1 wherein said electrical entry and exit ports of said electrically insulating interposer comprise copper or tungsten arrays overlaid by palladium, gold, platinum, or platinum-rich alloy.

14. A method for the fabrication of a semiconductor assembly:
providing a semiconductor wafer comprising a plurality of undivided integrated circuit chips, each circuit chip having a plurality of metal contact pads as electrical entry and exit ports;
forming a planar array of solder balls attached to said contact pads of said plurality of chips on said semiconductor wafer so that each of said contact pads is contacted by one of said solder balls;
providing an interposer of electrically insulating material having first and second opposite surfaces and electrically conductive paths from said first surface to said second surface, forming electrical entry and exit ports on said insulating interposer;
aligning said interposer with said solder balls so that each port is placed into alignment with one of said solder balls on said semiconductor wafer;
contacting said ports and said solder balls;
applying radiant energy to said semiconductor wafer such that said wafer increases uniformly in temperature and transfers heat to said solder balls, causing the solder balls to reach a liquid state;
separately controlling the temperature of said interposer in order to minimize differences in thermal expansion;
removing said energy such that said solder balls cool and harden, forming physical bonds between said solder balls and said ports; and
separating the resulting composite structure into discrete chips.

15. A method for the fabrication fo a semiconductor assembly comprising:
providing a silicon semiconductor wafer comprising a plurality of undivided integrated circuit chips, each circuit chip having a plurality of metal contact pads as electrical entry and exit ports;
forming a first planar array of solder balls attached to said contact pads of said plurality of chips on said semiconductor wafer so that each of said contact pads is contacted by one of said solder balls;
providing an interposer of electrically insulating material having first and second opposite surfaces and electrically conductive paths from said first surface to said second surface, forming electrical entry and exit ports on said insulating interposer;
aligning said interposer with said solder ball so that each port is placed into alignment with one of said solder balls on said semiconductor wafer;
contacting said ports and said solder balls;

applying radiant energy having a wavelength of 0.8 to 2.8 μm to said semiconductor wafer such that said wafer increases uniformly in temperature and transfers heat to said solder balls, causing said solder balls to reach a liquid state;
said wavelength causing the water to heat more rapidly than said interposer;
removing said energy such that said solder balls cool and harden, forming physical bonds between said solder balls and said ports;
forming a second planar array of solder balls attached to said exit ports of said interposer so that each of said exit ports is contacted by one of said solder balls; and
separating the resulting composite structure into discrete chips.

16. A method for the fabrication of a semiconductor assembly comprising:
providing a semiconductor wafer comprising a plurality of undivided integrated circuit chips, each circuit chip having a plurality of metal contact pads as electrical entry and exit ports;
providing an adhesive layer having first and second opposite surfaces and a multitude of electrically conductive fibers extending through electrically nonconductive material from said first surface to said second surface of the layer while remaining insulated from adjacent fibers;
providing an interposer of electrically insulating material having first and second opposite surfaces and electrically conductive paths from said first surface to said second surface, forming electrical entry and exit ports on said insulating interposer;
placing said interposer vertically and in contact with said adhesive substrate;
providing a polymer film having a plurality of discrete adhesive areas;
providing a plurality of solder balls, one of said solder balls being placed on each of said adhesive areas;
aligning said polymer film to said interposer so that each of said solder balls is placed into alignment with one of said ports;
placing said solder balls inc contact with said ports;
applying radiant energy to said semiconductor wafer such that said wafer uniformly increases in temperature and transfer heat to said adhesive substrate, said interposer and said solder balls, causing solder balls to reach a liquid state;
separately controlling the temperature of said interposer in order to minimize differences in thermal expansion;
removing said energy such that all said contacts form physical bonds and said solder balls cool and harden, forming physical bonds between said solder balls and said ports;
removing said polymer film; and
separating the resulting composite structure into discrete chips.

17. The method according to Claim 14, Claim 15, and Claim 16, wherein said solder balls comprise at least one alloy with a melting temperature compatible with multiple reflow.

18. The method according to Claim 14, Claim 15, and Claim 16, wherein said wafer contact pads, said solder balls, and said interposer ports comprise a combination of materials such that metal interdiffusion is minimized.

19. A method as in claim 14, further including the step of preheating said interposer prior to alignment with the wafer.

20. A method as in claim 15, further including the step of preheating said interposer prior to alignment with the wafer.